Remarks

The following remarks are responsive to the Office Action dated April 6, 2004. Applicants respectfully request the Examiner's reconsideration of the present application as amended.

Claims 1-9 have been cancelled. Claims 10-16 remain in the application and have been amended. No new matter has been added.

Drawings

The drawings are objected to under 37 CFR § 1.83(a). Applicants submit the enclosed drawing changes to conform with Examiner's suggestion. Enclosed herewith are marked up drawings with corrections and additions circled in red ink and a replacement set of formal drawings. No new matter has been added by these drawing amendments as described supra.

35 USC § 112 paragraph 2

Claims 1-16 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as their invention. The Examiner asserts that the limitations of claim 1 reads on a circuit arrangement that is not included in a drawing. Figures 2 and 3 have been amended to include a data output of each flip-flop connected to a gate of a corresponding transistor switch.

In addition, claims 10-16 have been amended to overcome the Examiner's antecedent basis rejections and to improve clarity.

Applicants therefore, respectfully submit that the claims, as amended, along with the drawing amendments, overcome any indefiniteness and antecedent basis rejections.

35 USC § 102(b)

The Examiner asserts that claims 1-14 are is rejected under 35 USC § 102(b) as being anticipated by U.S. Patent No. 5,708,455 to Maekawa, dated July 7, 1992. Claims 1-9 are cancelled.

Regarding Independent Claim 10

Maekawa discloses a shift register apparatus comprising unit registers, clocks, and gates. Maekawa describes an active matrix display device including at least one unit register having a data input, a data output, and a control clock. Unit registers are consecutively connected within a shift register that are driven by clock signals selectively shaped by gates and transistor switches.

The problem to be solved in Maekawa is to reduce the capacitive load on the clock lines and to achieve lower power consumption. In contrast, the problem to be solved by Applicants' invention is a circuit for fine-tuning a voltage output used to test or fine-tune an integrated circuit.

Maekawa discloses transfer gates connected to portions of the shift register. However, the transfer gates operate only to provide shaped clock pulses to the input of each unit register. Additionally, Maekawa discloses logic circuits that are used only to provide shaped clock pulses to the input of each unit register. In other words, any of the gates or switching transistors connected to the shift register in Maekawa are in the circuitry only to shape clock pulses that are applied to the input of each unit register.

In contrast, Applicants couple the output of each flip-flop to switching transistors that are coupled to a plurality of parallel resistors to fine-tune a voltage output. The switching transistors are configured to couple a corresponding resistor to ground depending on the logic state of a corresponding flip-flop. The logic state of the output from each flip-flop controls the conduction state of each

switching transistor, coupling each resistor to ground depending on the states in the flip-flops.

The flip-flop output logic states fine-tune the value of voltage output depending on the over-all resistance of the parallel resistor configuration. Specifically, Maekawa does not disclose or suggest the elements of claim 10, such as "*a plurality of resistors coupled in parallel to a voltage output.*" In addition, Maekawa does not disclose or suggest "*resistors coupled to ground through a corresponding plurality of switching transistors*", nor does Maekawa disclose or suggest that "*one or more resistors coupled to ground as determined by the states in said flip-flops.*"

Applicants therefore respectfully submit that claim 10 is patentable over Maekawa. Further, since claims 11-14 depend directly or indirectly from claim 10, they too are allowable for at least the same reasons. Accordingly, Applicants respectfully request that the Examiner withdraw the 35 USC § 102(b) rejections on claims 10-14.

In view of the foregoing amendment and remarks, Applicants respectfully submit that all the rejections and objections have been overcome. Accordingly, Applicants respectfully submit that amended claims 10-16 are in condition of allowance.

If a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact Applicants' representative at the number provided below.

CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Signed: Sally Azevedo
Typed Name: Sally Azevedo

Date: June 23, 2004

Respectfully submitted,

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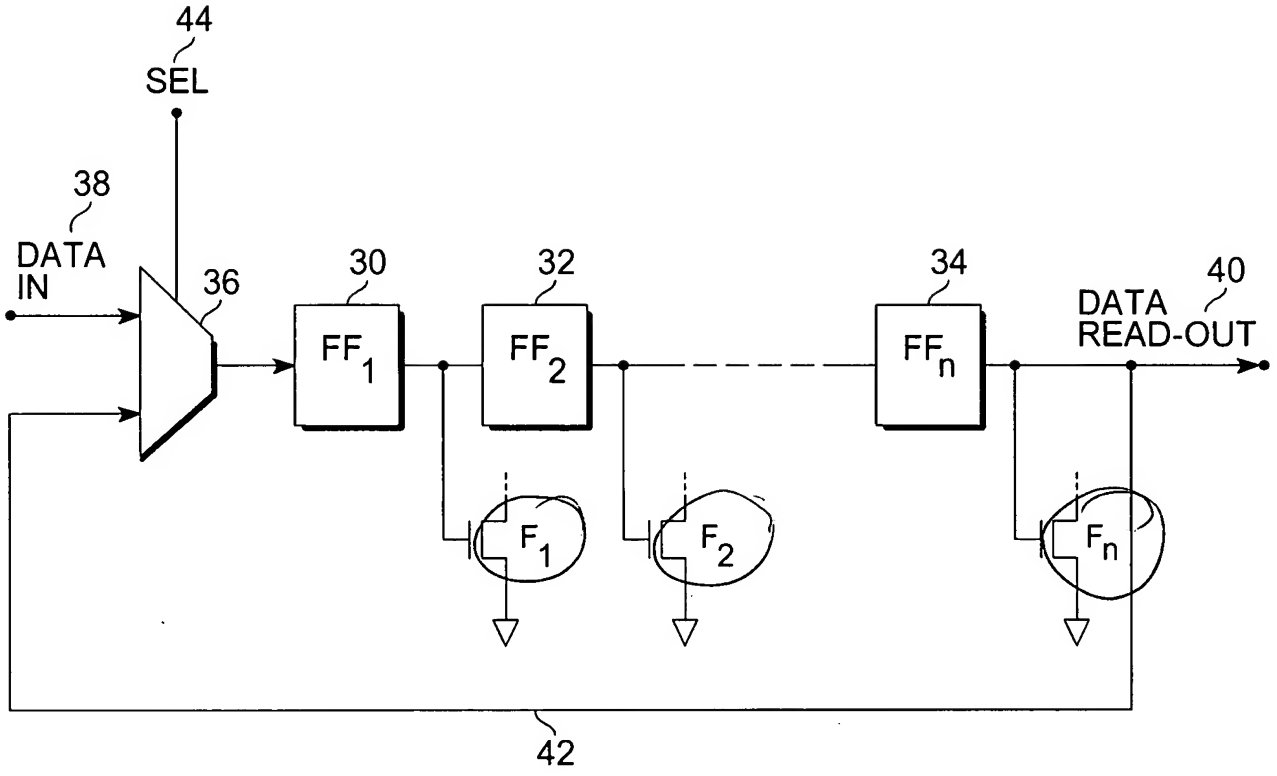
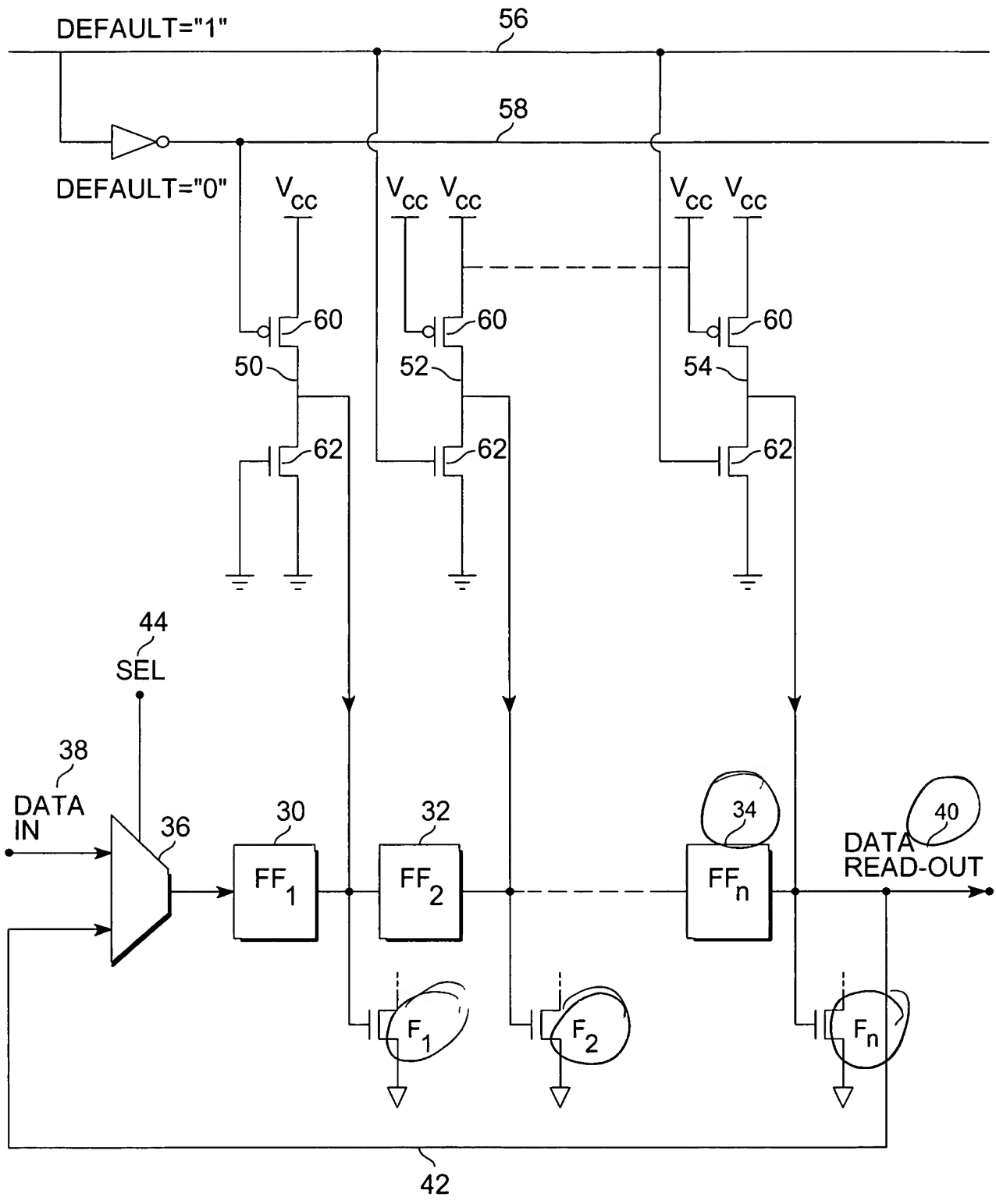


Fig._2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34
40
DATA READ-OUT
FF_1
FF_2
FF_n
F_1
F_2
F_n
42

Fig._3